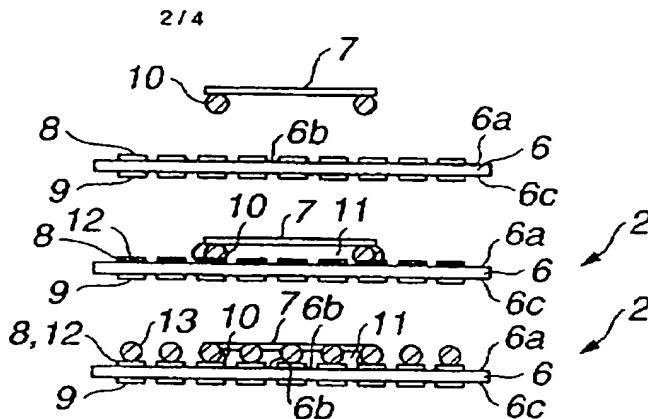
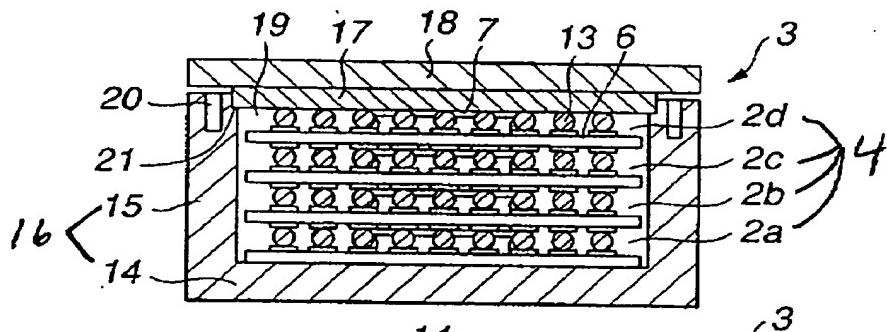
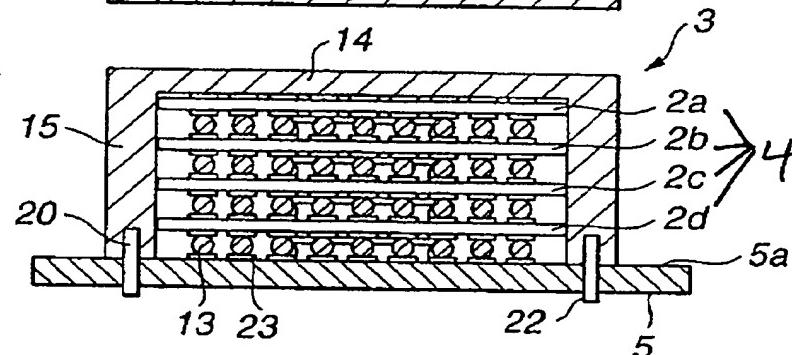
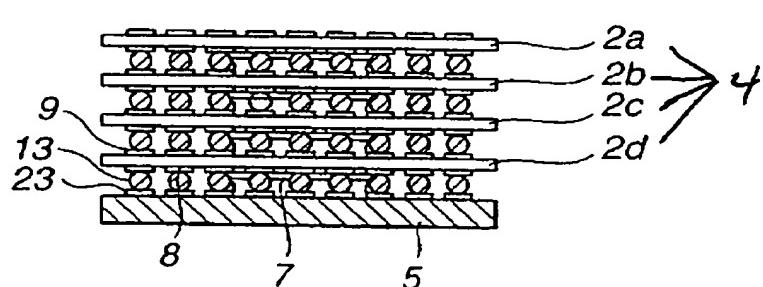
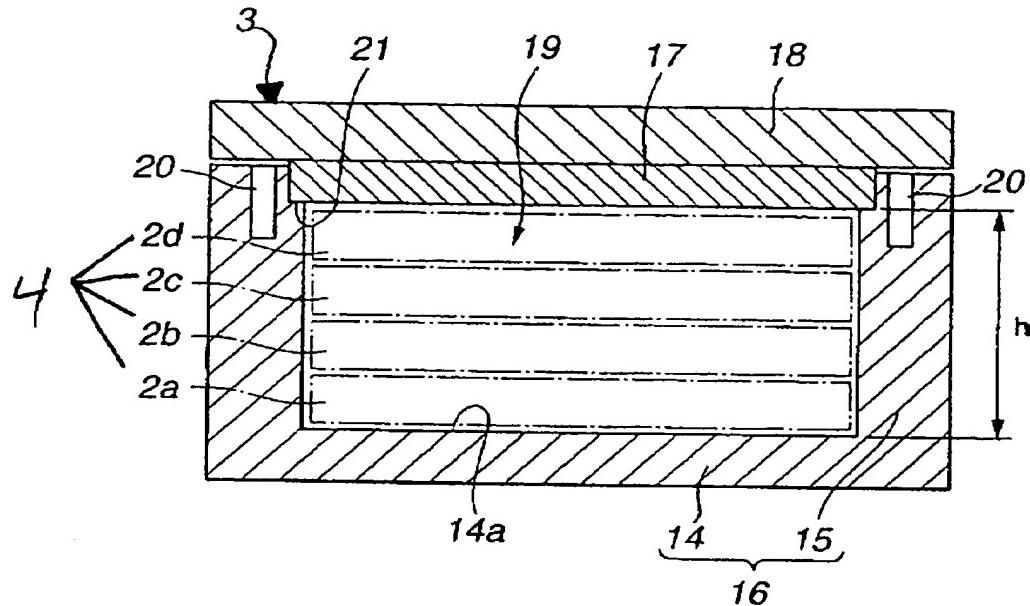
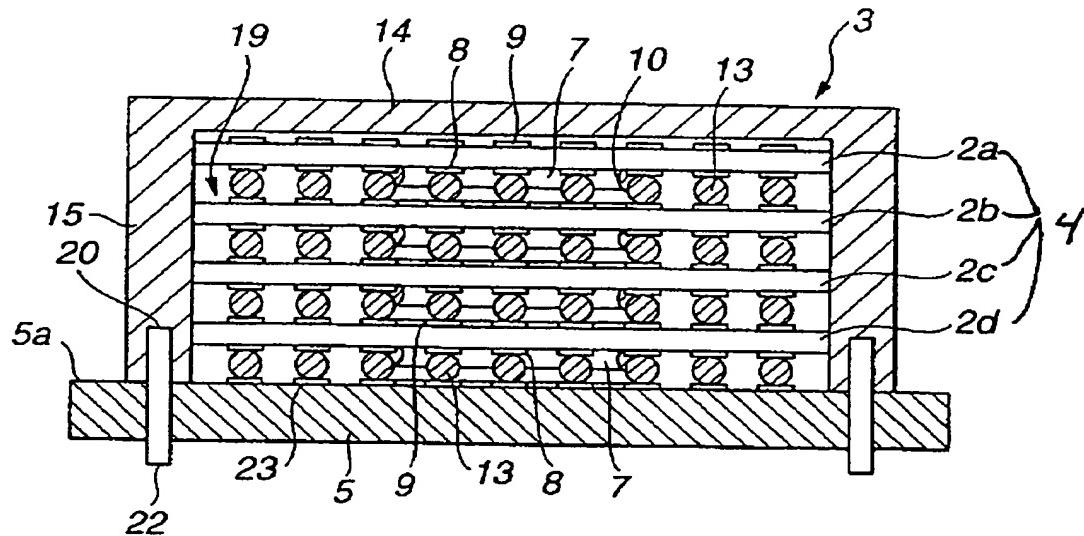


ASSEMBLY JIG AND MANUFACTURING METHOD OF MULTILAYER SEMICONDUCTOR DEVICE
 REPLACEMENT DRAWINGS Inventor: Yoshiyuki Yanagisawa et al.
 Serial No. 09/876,290
 Robert J. Depke, Holland & Knight LLP - (312) 263-3600

FIG.2(a)**FIG.2(b)****FIG.2(c)****FIG.2(d)****FIG.2(e)****FIG.2 (f)**

ASSEMBLY JIG AND MANUFACTURING METHOD OF MULTILAYER SEMICONDUCTOR DEVICE
 REPLACEMENT DRAWINGS Inventor: Yoshiyuki Yanagisawa et al.
 Serial No. 09/876,290
 Robert J. Depke, Holland & Knight LLP • (312) 263-3600

3 / 4

**FIG. 3****FIG. 4**

**ASSEMBLY JIG AND MANUFACTURING METHOD OF MULTILAYER SEMICONDUCTOR DEVICE
REPLACEMENT DRAWINGS**
Inventor: Yoshiyuki Yanagisawa et al.
Serial No. 09/676,290

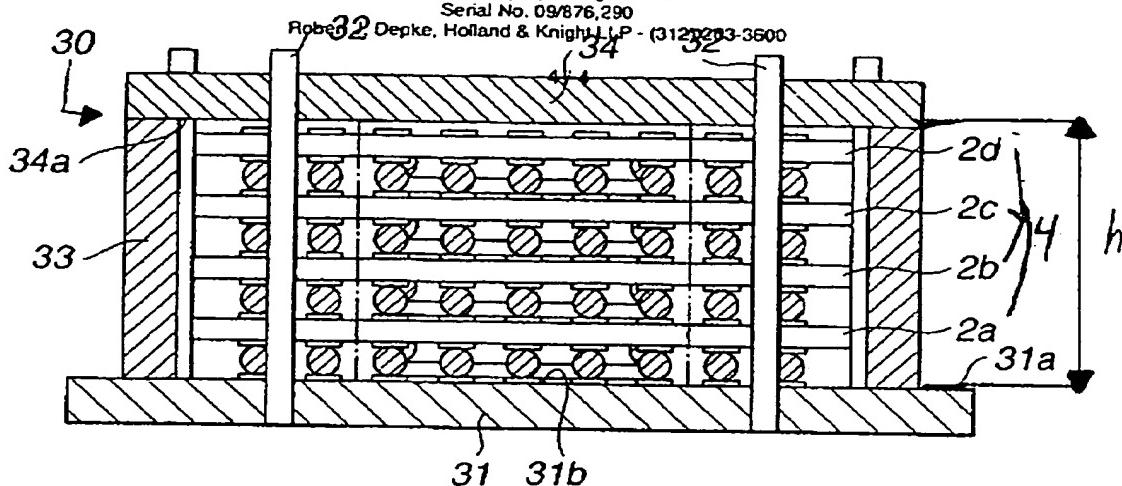


FIG.5(a)

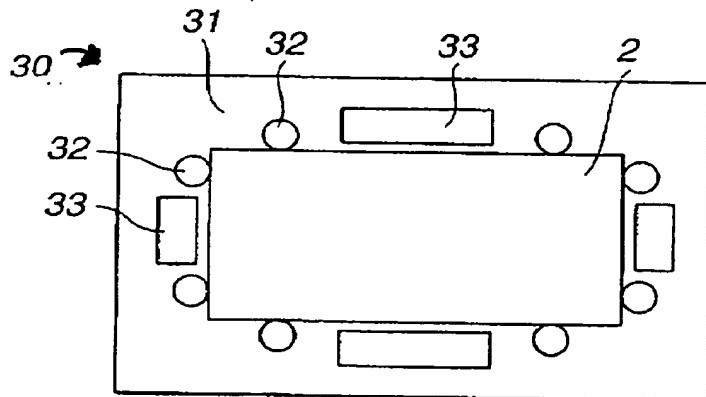


FIG.5(b)

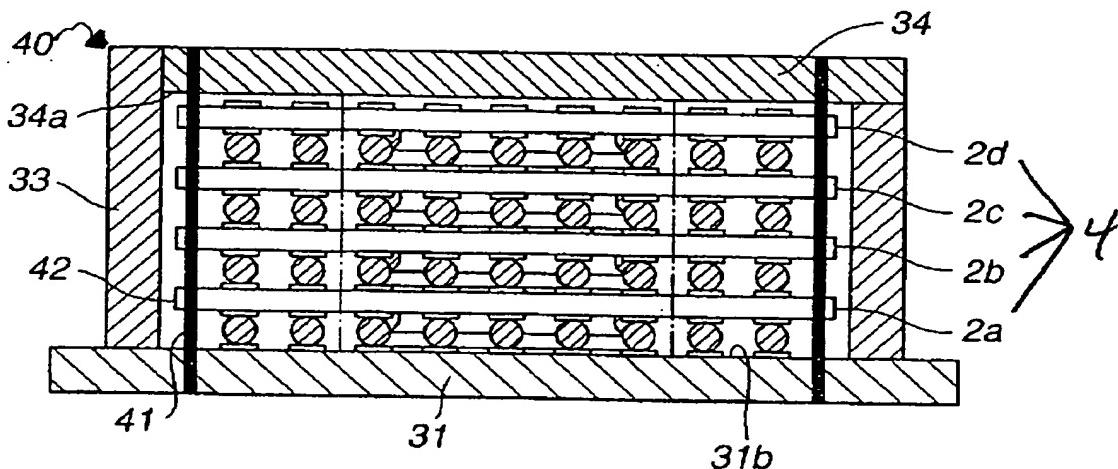


FIG.6